Basic circuit Concept

SHEET RESISTANCE *Rs*

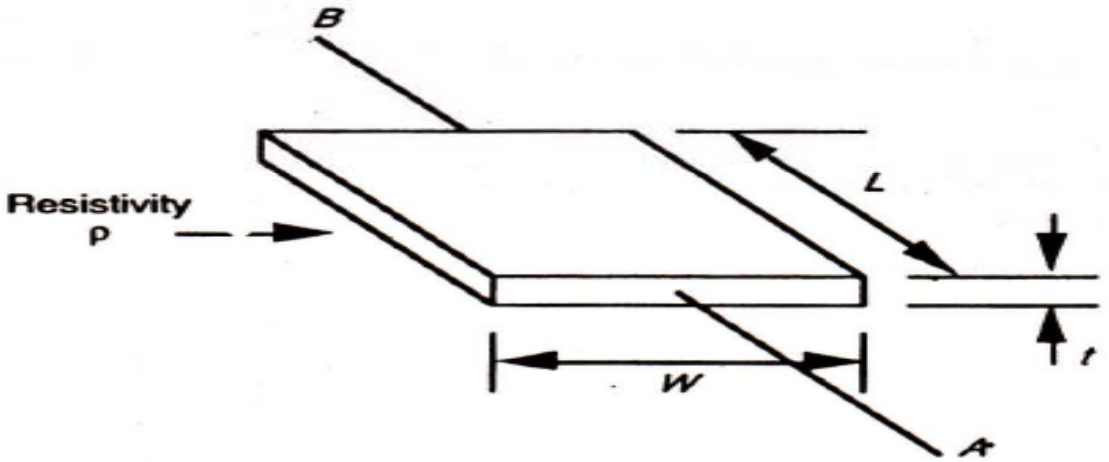


TABLE 4.1 Typical sheet resistances R_s of MOS layers for 5 μm*, and Orbit 2 μm* and 1.2 μm* technologies

Layer	*R_s ohm per square*		
	5 μm	*Orbit*	*Orbit 1.2 μm*
Metal	0.03	0.04	0.04
Diffusion (or active)**	10→50	20→45	20→45
Silicide	2→4	—	—
Polysilicon	15→100	15→30	15→30
n-transistor channel	$10^{4\dagger}$	$2 \times 10^{4\dagger}$	$2 \times 10^{4\dagger}$
p-transistor channel	$2.5 \times 10^{4\dagger}$	$4.5 \times 10^{4\dagger}$	$4.5 \times 10^{4\dagger}$

AREA CAPACITANCES OF LAYERS

- it will be apparent that conducting layers are separated from the substrate and each other by insulating (dielectric) layers,
- thus parallel plate capacitive effects must be present and must be allowed for.
- For any layer, knowing the dielectric (silicon dioxide) thickness, we can calculate area capacitance as follows:

$$C = \frac{\varepsilon_0 \varepsilon_{ins} A}{D} \text{ farads}$$

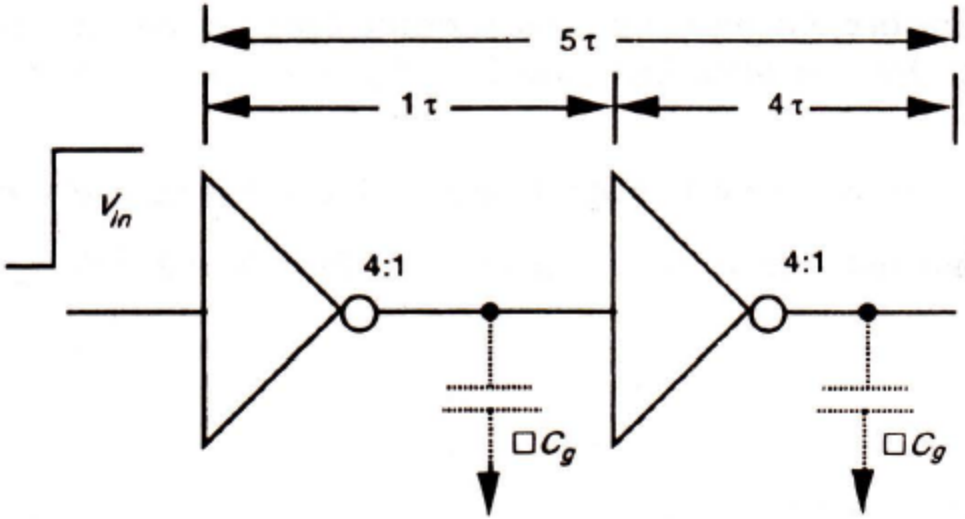
TABLE 4.2 Typical area capacitance values for MOS circuits

Capacitance	*Value in pF × $10^{-4}/\mu m^2$ (Relative values in brackets)*					
	5 μm		*2 μm*		*1.2 μm*	
Gate to channel	4	(1.0)	8	(1.0)	16	(1.0)
Diffusion (active)	1	(0.25)	1.75	(0.22)	3.75	(0.23)
Polysilicon* to substrate	0.4	(0.1)	0.6	(0.075)	0.6	(0.038)
Metal 1 to substrate	0.3	(0.075)	0.33	(0.04)	0.33	(0.02)
Metal 2 to substrate	0.2	(0.05)	0.17	(0.02)	0.17	(0.01)
Metal 2 to metal 1	0.4	(0.1)	0.5	(0.06)	0.5	(0.03)
Metal 2 to polysilicon	0.3	(0.075)	0.3	(0.038)	0.3	(0.018)

THE DELAY UNIT τ

Since the transition point of an inverter or gate is 0.5 *VDD• which is close to 0.63 VDD•* it appears to be common practice to use transit time and time constant (as defined for the delay unit t) interchangeably and 'stray' capacitances are usually allowed for by doubling (or more) the theoretical values calculated.

INVERTER DELAYS

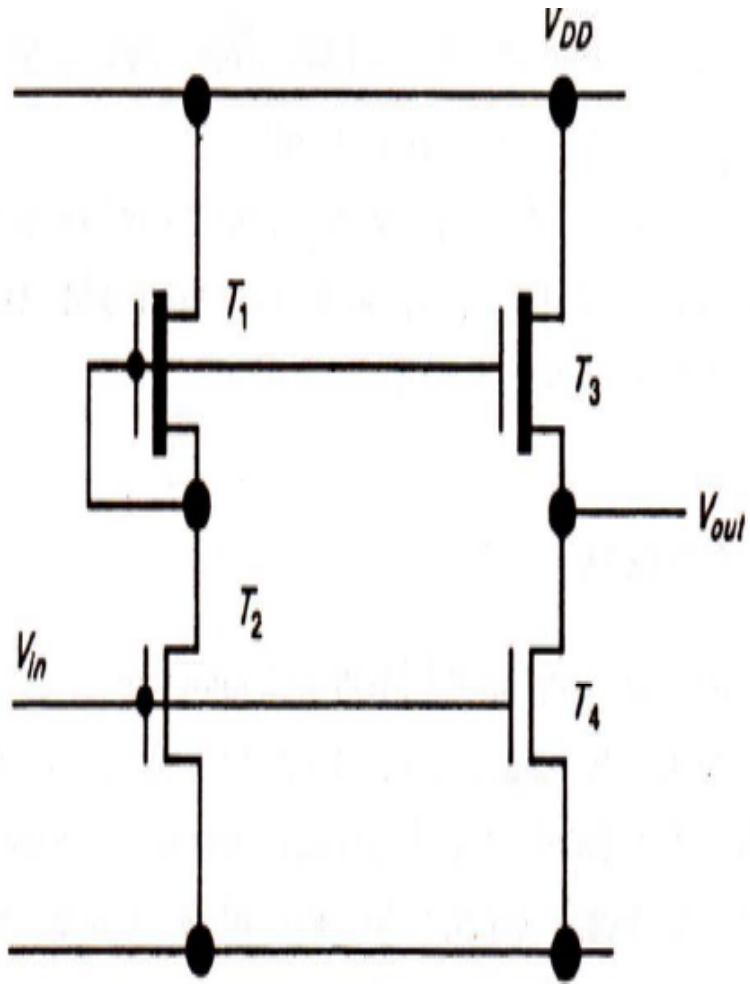


$$T_d = (1 + Z_{p.u.}/Z_{p.d.})\tau$$

Thus, the inverter pair delay for inverters having 4:1 ratio is 5τ.

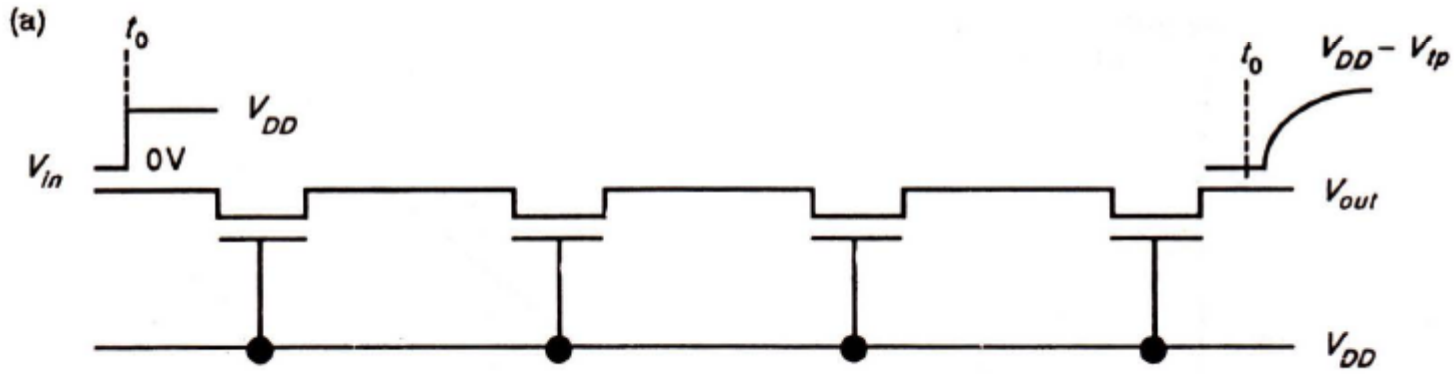
However, a single 4:1 inverter exhibits undesirable asymmetric delays since the delay in turning on is, for example, τ, while the corresponding delay in turning off is 4τ. Quite obviously, the asymmetry is worse when considering an inverter with an 8:1 ratio.

Super Buffers



considering a positive going logic transition *Vin at the input, it will be seen that the inverter formed by T1 and T2 is turned on and, thus,*
the gate of T3 is pulled down toward 0 volt with a small delay. Thus, T3 is cut off while *T4*
(the gate of which is also connected to *V;n) is turned on and the output is pulled down* qu'ickly.
Now consider the opposite transition: when *V;n drops to 0 volt, then the gate of T3 is* allowed to rise quickly to *V DD· Thus, as T4 is also turned off by Vin• T3 is made to conduct*

PROPAGATION DELAYS



the overall delay increases rapidly as *n increases and in practice no more than four pass* transistors should be normally connected in series. However, this number can be exceeded if a buffer is inserted between each group of four pass transistors *or if relatively long time* delays are acceptable.